REMARKS

1, 2. The specification is amended in response to the Examiner's objections. No new matter is added.

3-24. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent 5,220,512 (WATKINS). In response to this rejection, claims 4, 5, 16, and 17 are canceled and claims 1 - 3, 6 - 15, and 18 - 24 are amended. The following comments distinguish the claims, as amended, over WATKINS.

The invention relates to generating a display characterizing both the logic relationships and the temporal behavior of signals within a circuit. Prior art schematic diagrams characterize the logical relationships between signals within a circuit. For example in WATKINS' FIG. 4, XOR gate 308 symbolically characterizes logical relationships between the Q output of gates 304 and 306 and the U4 output of XOR gate 308. But schematic diagrams typically do not directly characterize how the signals of a circuit change over time. Prior art waveform diagrams and state tables characterize the temporal behavior of signals, but they do not show how the signals are logically interrelated. Thus in order for a circuit designer to determine why a particular signal took on a particular state at a particular time, he or she would have to look at both a schematic and a state table (or set of waveform diagrams) and figure out how the particular signal is logically related to other signals, and how state changes in those signals at earlier times affected the particular signal of interest at the particular time. This kind of analysis is very difficult.

WATKINS helps the designer a little by putting the waveform diagrams, the state table and the schematic diagram all in the same display as shown in FIG. 4. But the designer still can't easily figure out from this diagram how a state change in a signal at any one time is influenced by state changes in other signals at earlier times. The information that the designer needs to make such an analysis is contained in FIG. 4 but it is not in a form that makes it easy to perform the analysis.

The applicant's invention makes this kind of temporal "fan-in" analysis easier by more closely merging the information included in

the schematic diagram and the state table. Referring to the applicant's FIG 10, the applicant's display includes several columns of register symbols, wherein successive columns of register symbols correspond to successive times, in turn corresponding to successive edges of the clock signal that clocks the registers. Each register symbol in each column indicates a state of a register output signal of a separate register at a time corresponding to that column. Thus the array of register symbols includes basically the same information as the state table of WATKINS' FIG. 4.

However the applicant's display also includes a plurality of graphic symbols (lines), each visually linking one register symbol in one column corresponding to one time to other register symbols in another column corresponding to a preceding time. For example as shown in FIG. 10, lines link the symbol for register R1 in the column associated with time 90 to the symbols for registers R2 and R3 in the column associated with time 80. These lines indicate that the state of the output signal of register R1 at time 90 is a logical function of the states of the output signals of registers R2 and R3 at time 80. Note that other lines in the display show how register output signals at times 70 affected the states of output signals of registers R2 and R3 at time 80. This display makes it very easy for a circuit designer to work back in time to determine which signal states at any earlier time had an influence on the state of the output signal of register R1 at time 90.

It is much more difficult and time consuming for a designer to make this kind of determination from a display similar to WATKINS' FIG. 4.

Claim 1

Claim 1 (as amended) recites a step of generating a display of a plurality of columns of register symbols. Each successive column of register symbols corresponds to a successive time of occurrence of a clock signal edge. Each register symbol in each column indicates a state of a register output signal of a separate register at a time corresponding to that column. The Examiner correctly points out that applicant's "plurality of register symbols arranged in a plurality of columns" is somewhat similar to WATKINS' state table.

However claim 1 further recites "wherein the display also includes a graphical representation of a logical relationship depicted by one of the net models visually linking one register symbol of the register symbols residing in one of the columns to other register symbols residing in another of the columns, and wherein the graphical representation indicates that a register output signal state indicated by the one register symbol, and states of register output signals indicated by the other register symbols are logically interrelated." WATKINS does not teach visually linking any of the symbols of his state table to indicate logical relationships between the signals. To determine these logical relationships, the viewer must look at WATKINS' schematic diagram.

Thus the applicant's claim 1 as amended is patentable over WATKINS because WATKINS fails to teach the recited graphical representation visually linking register symbols in separate columns of his state table to indicate logical relationships between register output signal states.

Claim 13

Claim 13 (as amended) recites an apparatus to create displays described in applicant's claim 1. While, as the examiner has stated, the displayed WATKINS' data is similar to applicant's displays, the applicant's apparatus creates displays that are patently distinguishable from those of WATKINS and therefore applicant's required apparatus necessary to produce the patently distinguishable displays is also a patently distinguishable apparatus. Thus the applicant's claim 13 as amended is patentable over WATKINS because WATKINS apparatus to display a state table and a separate circuit model fails to teach an apparatus to create the recited graphical representation visually linking states of signals displayed as register symbols in separate columns representing the time of occurrence corresponding to the column in which they reside.

Claims 2 and 14

Claims 2 and 14 (as amended) depend on claims 1 and 13 respectively and are patentable over WATKINS for similar reasons. Claim 2 further recites, "The method in accordance with claim 1 wherein the state of the register output signal indicated by the one

register symbol is a function of the state of the register output signals indicated by the other register symbols." Applicant displays states of registers in columns corresponding to times of the clock signal edges and further displays, through the graphical representations visually linking the registers, a functional relationship between displayed register states in a succession of the columns. The state of a register output signal indicated by the one register symbol of claim 2 depicts how the "fan-in" of a state of a chosen register at a time represented by a chosen column is a function of other register states occurring at other times represented by other columns. This display, using applicant's FIG. 13 as an example, merges the information included in the schematic diagram of applicant's FIG. 1, and the state table similar to WATKINS FIG. 4. While WATKINS links logic devices, it does not teach displaying a graphical representation of the functional relationship visually linking the states of registers, indicated by register symbols, in columns corresponding to a time of occurrence. That is, WATKINS does not teach a graphical representation visually linking any of the symbols, representing states on the WATKINS state table, to indicate a functional relationships between the signal states.

Further applicant's claim 14 as amended is patentable over WATKINS because WATKINS fails to teach an apparatus to create the recited graphical representation visually linking the functional relationship between the states of registers, indicated by register symbols, in columns corresponding to a time of occurrence.

Claims 3 and 15

Claims 3 and 15 (as amended) depend on claims 1 and 13 respectively and are patentable over WATKINS for similar reasons. Claim 3 further recites, "The method in accordance with claim 1 wherein states of the register output signals indicated by the other register symbols are functions of the register output signal indicated by the one register symbol." Applicant displays states of registers in columns corresponding to times of clock signal edges and further displays, through the graphic representations visually linking the registers, a functional relationship between displayed register states in a succession of the columns. The state of the register output signal indicated by the one register symbol of claim 3 depicts how the

"fan-out" of a state of a chosen register at a time represented by a chosen column changes the states of other register states occurring at other times represented by other columns. This display, using applicant's FIG. 16 as an example, merges the information included in the schematic diagram of applicant's FIG. 1, and the state table similar to WATKINS FIG. 4. While WATKINS links logic devices, it does not teach displaying a graphical representation of the functional relationship visually linking the states of registers in columns corresponding to a time of occurrence. That is, WATKINS does not teach a graphical representation visually linking any of the symbols, representing states on the WATKINS state table, to indicate a functional relationships between the signal states.

Further applicant's claim 15 as amended is patentable over WATKINS because WATKINS fails to teach an apparatus to create the recited graphical representation visually linking the functional relationship between the states of registers, indicated by register symbols, in columns corresponding to a time of occurrence.

Claim 4

Claim 4 (as amended) depends on claim 1 and is patentable over WATKINS for similar reasons. Claim 4 adds, "... the display also includes a plurality of circuit input signal symbols arranged in at least one of the columns ..." and that the graphical representation visually links the circuit input signal symbols to other register symbols. Thus the applicant's claim 4 as amended is patentable over WATKINS because WATKINS fails to teach the recited graphical representation visually linking circuit input signal symbols placed in columns indicating a time of occurrence for each circuit input signal state, to the register symbols.

Claim 5 is cancelled.

Claim 6

Claim 6 (as amended) depends on claim 4 and is patentable over WATKINS for similar reasons. Claim 6 as dependent on claim 4 claims the graphical representation visually linking the register symbols to indicate a logical function between a register signal state, indicated by the register symbol, and "...indicates that the register output

signal state indicated by the one register symbol is a logical function of states of register output signals indicated by the other register symbols and the state of at least one of the circuit input signals." Applicant's displays indicate a logical function by displaying a graphical representation visually linking a circuit input signal symbol to a register symbol, in FIG. 14.

WATKINS does not teach a logical relationship by displaying a graphical representation visually linking the symbols of his state table to his schematic logic model. To determine these logical relationships, the viewer must look at WATKINS' separate schematic diagram and separate state table. Thus the applicant's claim 6 as amended is patentable over WATKINS because WATKINS fails to teach the recited logical relationships represented by the graphical representation visually linking register symbols indicating a time for the register signal state corresponding to the column where each register symbol resides, to circuit input signal symbols indicating a time for the circuit input signal state corresponding to the column where each circuit input signal symbol resides.

Claims 7 and 19

Claims 7 and 19 (as amended) depend on claims 1 and 13 respectively and are patentable over WATKINS for similar reasons. Claim 7 claims the specific limitation of lines as the graphical representation visually linking register symbols in separate columns to represent a logical relationship. Applicant's claim 7 as amended is patentable over WATKINS because WATKINS fails to teach lines as a graphical representation visually linking register symbols in separate columns to indicate logical relationships between register output signal states.

Further applicant's claim 19 as amended is patentable over WATKINS because WATKINS fails to teach an apparatus to create the lines as a graphical representation visually linking register symbols in separate columns to indicate logical relationships between register output signal states.

Claims 8 and 20

Claims 8 and 20 (as amended) depend on claims 1 and 13 respectively and are patentable over WATKINS for similar reasons.

Claim 8 claims a display depicting a graphical representation of one of the net models visually linking the circuit logic depicted by at least one of a plurality of logic gate symbols to the one register symbol. The register symbol resides in one of the columns corresponding to the time of occurrence of the state of register signal. These displays are illustrated in applicant's FIGS. 12, 13, 14 and 16. Applicant's claim 8 as amended is patentable over WATKINS because WATKINS fails to teach a display depicting a graphical representation of one of the net models visually linking the circuit logic depicted by at least one of a plurality of logic gate symbols to the one register symbol.

Further applicant's claim 20 as amended is patentable over WATKINS because WATKINS fails to teach an apparatus to create a display depicting a graphical representation of one of the net models visually linking the circuit logic depicted by at least one of a plurality of logic gate symbols to the one register symbol.

Claim 9

Claim 9 (as amended) depends on claim 6 and is patentable over WATKINS for similar reasons. Claim 9 claims the specific limitation of the representation of a logical relationship comprising lines interconnecting register symbols in separate columns and at least one of the circuit input signal symbols. Applicant's claim 6 as amended is patentable over WATKINS because WATKINS fails to teach the graphical representation of lines visually linking register symbols in separate columns to circuit input signal symbols where the lines indicate logical relationships between register output signal states and the state of at least one of the circuit input signals.

Claim 10

Claim 10 (as amended) depends on claim 6 and is patentable over WATKINS for similar reasons. Claim 10 claims a display indicating a logical relationship by depicting a graphical relationship visually linking register symbols and at least one circuit input signal symbol, to a register input signal symbol. The register symbols, the circuit input signal symbol, and the register input signal symbol resides in the column corresponding to the time of occurrence of the state of each register signal. This display is illustrated in applicant's FIG.

14 illustrating the logical relationship between the states of register signals and the states of at least one circuit input signal, to the state of a register input signal. Applicant's claim 10 as amended is patentable over WATKINS because WATKINS fails to teach representation of a logical relationship by displaying the recited graphical representation visually linking register symbols and the circuit input signal symbol in columns corresponding to the time of occurrence of the state of each signal, to a register input signal symbol.

Claim 11

Claim 11 (as amended) depends on claim 2 and is patentable over WATKINS for similar reasons. Claim 11 claims a distinguishable graphical representation visually linking the other register symbols to the one register symbol to indicate a changed state of the other register symbol. The state of the register output signal indicated by the one register symbol is a function of the state of the register output signals indicated by the other register symbols. This claim limitation is displayed in applicant's FIG. 11 where the distinguishable graphical representations are bold lines indicating the state of at least one of the register output signals is actively changing state. Applicant's claim 11 as amended is patentable over WATKINS because WATKINS fails to teach a distinguishable graphical representation visually linking one register symbol to indicate a changed state of another register symbol.

Claim 12

Claim 12 (as amended) recites a step of generating a display of a plurality of columns of symbols. Each symbol within each column indicates a state of a separate data signal. Each successive column of symbols corresponds to a successive time of occurrence of a clock signal edge. Each symbol in each column indicates a state of a data signal at a time corresponding to that column. The Examiner correctly points out that in WATKINS "... the position of the register state symbols represents a time occurrence of a clocked pulse signal edge ..." such that a plurality of columns of symbols in applicant's invention is somewhat similar to WATKINS' state table.

However claim 12 further includes the step of "displaying a graphical representation visually linking one symbol residing in one of the columns to others of the symbols residing in another of the columns, wherein the graphical representation indicates that a state of a data signal indicated by the one symbol, and states of data signals indicated by the others of the symbols are logically interrelated." WATKINS does not teach a graphical representation visually linking any of the symbols of his state table to indicate logical relationships between the signals. To determine these logical relationships, the viewer must look at WATKINS' schematic diagram.

Thus the applicant's claim 12 as amended is patentable over WATKINS because WATKINS fails to teach the recited graphical representation visually linking symbols in separate columns of his state table to indicate logical relationships between the states of data signals.

Claim 16

Claim 16 (as amended) depends on claim 13 and is patentable over WATKINS for similar reasons. Claim 16 claims an apparatus in which "... the display also includes a plurality of circuit input signal symbols arranged in at least one of the columns ..." and in which the graphical representation visually links the circuit input signal symbols to other register symbols. Thus the applicant's claim 16 as amended is patentable over WATKINS because WATKINS fails to teach an apparatus to create the recited graphical representation visually linking circuit input signal symbols placed in columns indicating a time of occurrence for each circuit input signal state, to the register symbols.

Claim 17 is cancelled.

Claim 18

Claim 18 (as amended) depends on claim 16 and is patentable over WATKINS for similar reasons. Claim 18 as dependent on claim 16 claims the graphical representation visually linking the register symbols to indicate a logical function between a register signal state, indicated by the register symbol, and "... a state of at least one of the circuit input signals depicted by a circuit input signal symbol." Applicant

displays the logical function through visually linking a circuit input signal symbol to a register symbol, in FIG. 14.

WATKINS does not teach an apparatus to display a logical relationship by displaying a graphical representation visually linking the symbols of his state table to his schematic logic model. To determine these logical relationships, the viewer must look at WATKINS' separate schematic diagram and separate state table. Thus the applicant's claim 18 as amended is patentable over WATKINS because WATKINS fails to teach an apparatus to create the recited graphical representation visually linking register symbols to indicate a logical function between a register signal state and a state of a circuit input signal depicted by a each circuit input signal symbol.

Claim 21

Claim 21 (as amended) depends on claim 18 and is patentable over WATKINS for similar reasons. Claim 21 claims an apparatus to create the specific limitation of lines indicating a logical relationship by displaying the graphical representation visually linking register symbols in separate columns to at least one of the circuit input signal symbols. Applicant's claim 21 as amended is patentable over WATKINS because WATKINS fails to teach an apparatus to create the graphical representation of lines visually linking register symbols in separate columns to circuit input signal symbols where the lines indicate logical relationships between register output signal states and the state of at least one of the circuit input signals.

Claim 22

Claim 22 (as amended) depends on claim 18 and is patentable over WATKINS for similar reasons. Claim 22 claims an apparatus to create a display indicating a logical relationship by depicting a graphical relationship visually linking register symbols and at least one circuit input signal symbol, to a register input signal symbol. The register symbols, the circuit input signal symbol, and the register input signal symbol reside in the columns corresponding to the time of occurrence of the state of each register signal. This display is illustrated in applicant's FIG. 14 illustrating the logical relationship between the states of register signals and the states of at least one circuit input signal, to the state of a register input

signal. Applicant's claim 22 as amended is patentable over WATKINS because WATKINS fails to teach an apparatus to create a logical relationship by displaying the recited graphical representation visually linking register symbols and the circuit input signal symbol in columns corresponding to the time of occurrence of the state of each signal, to a register input signal symbol.

Claim 23

Claim 23 (as amended) depends on claim 14 and is patentable over WATKINS for similar reasons. Claim 23 claims an apparatus to create a distinguishable graphical representation visually linking the other register symbols to the one register symbol to indicate a changed state of the other register symbol. The state of the register output signal indicated by the one register symbol is a function of the state of the register output signals indicated by the other register symbols. This claim limitation is displayed in applicant's FIG. 11 where the distinguishable graphical representations are bold lines indicating the state of at least one of the register output signals is actively changing state. Applicant's claim 11 as amended is patentable over WATKINS because WATKINS fails to teach an apparatus to create a distinguishable graphical representation visually linking one register symbol to indicate a changed state of another register symbol.

Claim 24

Claim 24 (as amended) recites an apparatus to generate a display of a plurality of columns of symbols. Each symbol within each column indicates a state of a separate a data signal. Each successive column of symbols corresponds to a successive time of occurrence of a clock signal edge. Each symbol in each column indicates a state of a data signal at a time corresponding to that column. The Examiner correctly points out in WATKINS that the position of the register state symbols represents a time of occurrence of a clocked pulse signal edge such that a plurality of columns of symbols in applicant's invention is somewhat similar to WATKINS' state table thus indicating applicant's and WATKINS' apparatus would be the same.

However claim 24 further includes an apparatus to display a graphical representation visually linking one symbol residing in one

of the columns to others of the symbols residing in another of the columns, wherein the graphical representation indicates that a state of a data signal indicated by the one symbol, and states of data signals indicated by the others of the symbols are logically interrelated. WATKINS does not teach an apparatus to create a display visually linking any of the symbols of his state table to indicate logical relationships between the signals. To determine these logical relationships, the viewer must look at WATKINS' schematic diagram.

Thus the applicant's claim 24 as amended is patentable over WATKINS because WATKINS fails to teach an apparatus to create the recited graphic representation visually linking symbols in separate columns of his state table to indicate logical relationships between the states of signals.

The additional prior art references cited by the Examiner have been reviewed and do not appear to disclose or suggest the invention as claimed.

In view of the forgoing amendments and remarks, it is believed the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

John Smith-Hill
Reg. No. 27,730

SMITH-HILL & BEDELL, P.C.
12670 NW Barnes Road, Suite 104
Portland, Oregon 97229

Tel. (503) 574-3100
Fax (503) 574-3197
Docket: NOVA 2198

Certificate of Facsimile Transmission

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

John Smith-Hill

12/14/04
Date